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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
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09/392,034 09/08/99 GONZALEZ

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EXAMINER

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ART UNIT

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Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No. 09/392,034	Applicant(s) GONZALEZ ET AL.	
	Examiner Anh D. Mai	Art Unit 2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Status

- 1) ☒ Responsive to communication(s) filed on 30 May 2000.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-43 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-43 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are objected to by the Examiner.
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).
- a) ☐ All b) ☐ Some * c) ☐ None of the CERTIFIED copies of the priority documents have been:
1. ☐ received.
2. ☐ received in Application No. (Series Code / Serial Number) _____.
3. ☐ received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. & 119(e).

Attachment(s)

- 15) ☒ Notice of References Cited (PTO-892) 18) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 19) ☐ Notice of Informal Patent Application (PTO-152)
- 17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ 20) ☐ Other: _____

DETAILED ACTION

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

1. Claims 1-43 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-43 of U.S. Patent No. 5,953,621. Although the conflicting claims are not identical, they are not patentably distinct from each other because:

The process steps of present claims 1-43 are clearly directed to a method of forming a "trench isolation" since "semiconductor substrate, dielectric layer, trenches, etc.," as recited in claims 1, 7, 14, 18, 24-26, 28, 31, 35, 38 and 41-43 of Gonzalez '621, are obviously parts of a "microelectronic structure". The term "trench isolation" of '621 is recognized in the art to be a "microelectronic structure". Therefore, present claims 1-43 are obvious over claims 1-43 of '621.

Further, the term such as "wherein the microelectronic structure is defined at least in part by the plurality of spacers, the conformal third layer, and the plurality of

isolation trenches", is clearly an obvious variation of the "isolation trench structure is defined at least in part by the plurality of spacers, the conformal third layer, and the plurality of isolation trenches".

In fact, the additional of the term such as "wherein the microelectronic structure is defined at least in part by the plurality of spacers, the conformal third layer, and the plurality of isolation trenches" fails to further limit the scope of the claims 1-43 of '621.

Specification

2. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required:

The limitation such as: "wherein said upper surface for each said isolation trench is formed in an etch process using an etch recipe that etches said first dielectric layer *faster than* said conformal layer and said spacers by a ratio in range from of about 1:1 to about 2:1" fails to get support from the specification.

However, the specification discloses: a first preferred selectivity of an etch recipe used in the inventive method is in the range of about 1:1 to about 2:1, selective to *isolation film 36* as compared to insulator island 22. (See page 14, lines 18-22).

Thus, specification only provides support for etching of conformal layer faster than the first dielectric layer.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 4, 16, 23 is rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claim 16 recites: "wherein said liner is composed of silicon nitride" in addition to the limitations of claim 14 including: "forming a liner upon a sidewall of each said isolation trench, said liner extending from an interface thereof with said oxide layer to the termination of said isolation trench *within* said semiconductor substrate".

Since the formation of silicon nitride liner (30) is CVD, (See page 12, lines 14-24), the top surface (22) of layer (16) should be covered by the CVD silicon nitride (30). See Poon et al. (U.S. Patent No. 5,387,540).

How can a CVD silicon nitride layer only form on the trench surface?

Is this a selective deposition?

What are the deposition parameters that results in the silicon nitride liner only form on the trench surface?

Notice that silicon nitride and trench fill oxide are two completely different materials, therefore, they can not be assimilated at the end of the process as shown in Figs. 8A, 8B and 9A, 9B.

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The similar rejection also applies to claims 4, 23.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 32 and 33 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The term "*composed on*" is indefinite because: it is not clear whether applicant intended to claim "formed on" or "composed of".

The specification fails to support neither the second layer (36) "composed of" electrically conductive material nor the second layer (36) "formed on" a electrically conductive material.

Insofar as understood by examiner, the second layer is "composed of" a electrically conductive material.

5. Claims 9, 10, 12, 13, 26, 27, 29 and 30 recites the limitation, as an example claim 9, " wherein said upper surface for each said isolation trench is formed in an etch process using an etch recipe that etches said *first dielectric layer faster than said conformal layer and said spacers* by a ratio in range from of about 1:1 to about 2:1" in lines 1-4. There is insufficient antecedent basis for this limitation in the claim.

However, the specification discloses the opposite.

Claim R jections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

6. Claims 1 and 6 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Omid-Zohoor (U.S. Patent No. 6,097,072).

Omid-Zohoor teaches a method of forming a microelectronic structure as claimed including:

forming an oxide layer (340) upon a semiconductor substrate (120);

forming a first dielectric layer (344) upon the oxide layer;

selectively removing the first dielectric layer to exposed the oxide layer at a plurality of areas;

forming a second dielectric layer (352) conformally over the oxide layer and the first dielectric layer;

selectively removing the second dielectric layer to form a plurality of spacers (356) from the second dielectric layer, wherein each spacer is situated upon the oxide layer, is in contact with the first dielectric layer, and is adjacent to an area of the plurality of areas;

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forming a plurality of isolation trenches (360) extending below the oxide layer into the semiconductor substrate, wherein each the isolation trench is adjacent to and below a pair of the spacers and is situated at a corresponding area of the plurality of areas;

filling each the isolation trench with a conformal layer (364), the conformal layer extending above the oxide layer in contact with a corresponding pair of the spacers;

planarizing the conformal layer and each spacer to form therefrom an upper surface for each the isolation trench that is co-planar to the other the upper surfaces;

wherein material that is electrically insulative extends continuously between and within the plurality of isolation trenches. (See Figs. 3A-M, col. 4, l. 1-col. 5, l. 4).

With respect to claim 6, the upper surface for each isolation trench of Omid-Zohoor is formed by CMP.

7. Claims 7, 8 and 11 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Omid-Zohoor (U.S. Patent No. 6,097,072).

Omid-Zohoor teaches a method of forming a microelectronic structure as claimed including:

forming an oxide layer (340) upon a semiconductor substrate (120);

forming a first dielectric layer (344) upon the oxide layer;

selectively removing the first dielectric layer to exposed the oxide layer at a plurality of areas;

forming a second dielectric layer (352) conformally over the oxide layer and the first dielectric layer;

selectively removing the second dielectric layer to form a plurality of spacers (356) from the second dielectric layer, wherein each spacer is situated upon the oxide layer, is in contact with the first dielectric layer, and is adjacent to an area of the plurality of areas;

forming a plurality of isolation trenches (360) extending below the oxide layer into the semiconductor substrate, wherein each the isolation trench is adjacent to and below a pair of the spacers and is situated at a corresponding area of the plurality of areas;

filling each the isolation trench with a conformal layer (364), the conformal layer extending above the oxide layer in contact with a corresponding pair of the spacers;

planarizing the conformal layer and each spacer to form therefrom an upper surface for each the isolation trench that is co-planar to the other the upper surfaces, wherein:

material that is electrically insulative extends continuously between and within the plurality of isolation trenches;

the conformal layer and the spacers form the upper surface for each isolation trench, each upper surface being formed from the conformal layer and the spacer and being situated above the pad oxide layer; and

the first dielectric layer is in contact with at least a pair of the spacers and the pad oxide layer. (See Figs. 3A-M, col. 4, l. 1-col. 5, l. 4).

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With respect to claim 8, the method of Omid-Zohoor further includes:

removing the pad oxide layer upon portion of the surface of the semiconductor substrate; and

forming a gate oxide layer (380) upon the portion of the surface of the semiconductor substrate.

With respect to claim 11, the upper surface of each isolation trench of Omid-Zohoor is formed by the steps comprising:

CMP, wherein the conformal layer, the spacers and the first dielectric layer form a planar first upper surface; and

an etch the forms a second upper surface, the second upper surface being situated above the pad oxide layer. (See Fig. 3N).

8. Claim 38 is rejected under 35 U.S.C. 102(e) as being clearly anticipated by Omid-Zohoor (U.S. Patent No. 6,097,072).

Omid-Zohoor teaches a method of 4 forming a microelectronic structure, the method comprising:

providing a semiconductor substrate (120) having a top surface with an oxide layer (340) thereon;

forming a first layer (344) upon the oxide layer;

forming a plurality of isolation trenches (360) having electrically insulative material (364) extending continuously between and within the plurality of isolation trench, each isolation trench:

having a spacer (356) composed of dielectric material upon the oxide layer in contact with the first layer;

extending from an opening thereto at top surface of the semiconductor substrate and below the oxide layer into and terminating within the semiconductor substrate adjacent to and below the spacer;

having a second layer (364) filling the isolation trench and extending above the oxide layer in contact with the spacer; and

having planar upper surface formed from the second layer and the spacer and being situated above the oxide layer; and

wherein the microelectronic structure is defined at least in part by the plurality of spacers, the second layer, and the plurality of isolation trenches. (See Figs. 3A-M, col. 4, l. 1-col. 5, l. 4).

9. Claim 41 is rejected under 35 U.S.C. 102(e) as being clearly anticipated by Omid-Zohoor (U.S. Patent No. 6,097,072).

Omid-Zohoor teaches a method of forming a microelectronic structure as claimed including:

providing a semiconductor substrate (120) having a top surface;

forming first and second isolation trenches (360) each:

extending into and being defined by the semiconductor substrate;

having an opening thereto at the top surface of the semiconductor substrate; and

extending below and being centered between a pair of spacers (356) situated above the top surface of the semiconductor substrate; and wherein:

an electrically insulative material (364) extends continuously between and within the first and second isolation trenches; and

a planar surface begins at the first isolation trench and extends continuously to the second isolation trench;

wherein the microelectronic structure is defined at least in part by the pair of spacers, the electrically insulative material and the first and second isolation trenches. (See Figs. 3A-M, col. 4, l. 1-col. 5, l. 4).

10. Claim 43 is rejected under 35 U.S.C. 102(e) as being clearly anticipated by Omid-Zohoor (U.S. Patent No. 6,097,072).

Omid-Zohoor teaches a method of forming a microelectronic structure as claimed including:

providing a semiconductor substrate (120) having a top surface with an oxide layer (340) thereon;

forming a first layer (344) upon the oxide layer;

forming a first isolation structure including:

a first spacer (356) composed of a dielectric material upon the oxide layer in contact with the first layer;

a first isolation trench (356) extending from an opening thereto at the top surface of the semiconductor substrate and below the oxide layer into and terminating

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within the semiconductor substrate adjacent to and below the first spacer, wherein the first spacer is situated on a side of the first isolation trench;

a second spacer (356) composed of a dielectric material upon the oxide layer in contact with the first layer, the second spacer being situated on a side of the first isolation trench opposite the side of the first spacer;

forming a second isolation structure including:

a first spacer (356) composed of a dielectric material upon the oxide layer in contact with the first layer;

a first isolation trench (360) extending below the oxide layer into and terminating within the semiconductor substrate adjacent to and below the first spacer of the second isolation structure, wherein the first spacer of the second isolation structure is situated on a side of the first isolation trench;

a second spacer (356) composed of a dielectric material upon the oxide layer in contact with the first layer (344), the second spacer of the second isolation structure being situated on a side of the first isolation trench opposite the side of the first spacer of the second isolation structure;

forming an active area located within the semiconductor substrate between the first and second isolation structures;

forming a second layer (364), composed of an electrically insulative material, filling the first and second isolation trenches and extending continuously therebetween and above the oxide layer (340) in contact with the first and second spacers (356) of the respective first and second isolation structures; and forming a planar upper surface

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formed from the second layer (364) and the first and second spacers (356) of the respective first and second isolation structures, and being situated above the oxide layer, wherein the microelectronic structure is defined at least in part by the active area, the second layer, and the first and second isolation trenches. (See Figs. 3A-M, col. 4, l. 1-col. 5, l. 4).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

11. Claims 2-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Omid-Zohoor '072 as applied to claim 1 above and further in view of Poon et al. (U.S. Patent No. 5,387,540).

Omid-Zohoor is shown to teach all of the features of the claim with the exception of forming a liner upon a sidewall of the isolation trench (360).

However, Poon teaches forming liner (28) upon the sidewall (24) of the isolation trench (22). (See Fig. 4).

It would have been obvious to one having ordinary skill in the art at the time of the invention was made to form the liner (28) upon a sidewall of each isolation trench (360) of Omid-Zohoor as taught by Poon to release stress on the trench surface.

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With respect to claim 3, the liner (28) of Poon is thermally grown oxide of the semiconductor substrate.

With respect to claim 4, the liner (50) of Poon comprises deposition of a composition of matter. (See Fig. 11).

With respect to claim 5, Poon further teaches forming a doped region (30) below the termination of each isolation trench (22) within the semiconductor substrate (12). (See Fig. 4).

It would have been obvious to one having ordinary skill in the art at the time of the invention was made to form a doped region (30) below the termination of each isolation trench (360) within the semiconductor substrate (120) of Omid-Zohoor as taught by Poon to provide further electrical isolation effect between circuit components.

12. Claims 9, 10, 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Omid-Zohoor as applied to claim 7 above, and further in view of Lee '316.

Thus, Omid-Zohoor is shown to teach all of the features of the claim with the exception of using an etch recipe that etch the first dielectric layer (344) fast than the conformal layer (364) and the spacers (356).

However, Lee '316 teaches using an etch recipe that results in an upper surface for each isolation trench that is co-planar to the other the upper surfaces. (See Fig. 9).

It would have been obvious to one having ordinary skill in the art at the time of the invention was made to use the etch recipe during the planarization of the conformal

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layer (364) of Omid-Zohoor as taught by Lee '316 to form an isolation trench that is coplanar to the other upper surface.

Within purview of one having ordinary skill in the art, it would have been obvious to determine the optimum etch ratio of the layers. See *In re Aller*, Lacey and Hall (10 USPQ 233-237) "It is not inventive to discover optimum or workable ranges by routine experimentation."

13. Claims 14-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Omid-Zohoor '072 in view of Poon et al. (U.S. Patent No. 5,387,540).

Omid-Zohoor teaches a method of forming a microelectronic structure substantially as claimed including:

forming an oxide layer (340) upon a semiconductor substrate (120);

forming a silicon nitride layer (344) upon the oxide layer;

selectively removing the silicon nitride layer to exposed the oxide layer at a plurality of areas;

forming a first silicon dioxide layer (352) over the oxide layer and the silicon nitride layer;

selectively removing the first silicon dioxide layer to form a plurality of spacers (356) from the first silicon dioxide layer, wherein each spacer is situated upon the oxide layer, is in contact with the silicon nitride layer, and is adjacent to an area of the plurality of areas;

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forming a plurality of isolation trenches (360) extending below the oxide layer into and terminating within the semiconductor substrate, wherein each isolation trench is adjacent to and below a pair of the spacers and is situated at a corresponding area of the plurality of areas;

forming a corresponding electronically active region below the termination of each isolation trench within the semiconductor substrate;

filling each isolation trench with a second silicon dioxide layer (364), the second silicon dioxide layer within each isolation trench extending above the oxide layer in contact with a corresponding pair of the spacers; and

selectively removing the second silicon dioxide layer and the spacers to form an upper surface for each isolation trench that is co-planar to the other upper surfaces and being situated above the pad oxide layer, wherein material that is electrically insulative extends continuously between and within the plurality of isolation trenches. (See Figs. 3A-M, col. 4, l. 1-col. 5, l. 4).

Thus, Omid-Zohoor is shown to teach all of the features of the claim with the exception of forming a liner upon a sidewall of each isolation trench.

However, Poon teaches forming a trench liner (28) upon a sidewall of each isolation trench, the liner extending from an interface thereof with the oxide layer (14) to the termination of the isolation trench within the semiconductor substrate (12). (See Fig. 4).

It would have been obvious to one having ordinary skill in the art at the time of the invention was made to form the liner (28) upon a sidewall of each isolation trench (360) of Omid-Zohoor as taught by Poon to release stress on the trench surface.

With respect to claim 15, the liner (28) of Poon is thermally grown oxide of the semiconductor substrate.

With respect to claim 16, the liner (50) of Poon is composed of silicon nitride. (see Fig. 11).

With respect to claim 17, the method of Omid-Zohoor further includes:

removing the pad oxide layer upon portion of the surface of the semiconductor substrate; and

forming a gate oxide layer (380) upon the portion of the surface of the semiconductor substrate.

14. Claims 18-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Omid-Zohoor '072 in view of Lee '316.

Omid-Zohoor teaches a method of forming a microelectronic structure substantially as claimed including:

forming an oxide layer (340) upon a semiconductor substrate (120);

forming a first dielectric layer (344) over the semiconductor substrate;

selectively removing the first dielectric layer to expose the oxide layer at a plurality of areas;

forming a second dielectric layer (352) conformally over the oxide layer and the first dielectric layer;

selectively removing the second dielectric layer to form a plurality of spacers (356) from the second dielectric layer, wherein each the spacer is upon the oxide layer, is in contact with the first dielectric layer, and is adjacent to an area of the plurality of areas;

forming a plurality of isolation trenches (360) extending below the oxide layer into and terminating within the semiconductor substrate, wherein each the isolation trench is adjacent to and below a pair of the spacers and is situated at a corresponding area of the plurality of areas;

filling each the isolation trench with a conformal third layer (364), the conformal third layer extending above the oxide layer in contact with a corresponding pair of the spacers;

planarizing the conformal third layer to form therefrom an upper surface for each the isolation trench that is co-planar to the other the upper surfaces;

wherein material that is electrically insulative extends continuously between and within the plurality of isolation trenches;

wherein planarizing the conformal third layer to form therefrom the upper surface for each the isolation trench that is co-planar to the other the upper surfaces further comprises planarizing the conformal third layer and each the spacer to form therefrom the co-planar upper surfaces; and

wherein the microelectronic structure is defined at least in part by the plurality of

spacers, the conformal third layer and the plurality of isolation trenches. (See Figs. 3A-M, col. 4, l. 1-col. 5, l. 4).

Thus, Omid-Zohoor is shown to teach all of the features of the claim with the exception of forming a polysilicon layer upon the oxide layer (340).

However, Lee teaches forming a polysilicon layer (36) therebetween the oxide layer (34) and the first dielectric layer (38). (See Fig. 6).

It would have been obvious to one having ordinary skill in the art at the time of the invention was made to form a polysilicon layer (36) between the oxide layer (340) and the first dielectric layer (344) of Omid-Zohoor as taught by Lee to form an etch selectable layer that is differed from the oxide layer and the first dielectric layer.

With respect to claim 19, the upper surface of each isolation trench is formed by CMP.

With respect to claim 20, Lee further teaches forming a doped region (26) below the termination of each isolation trench (22) within the semiconductor substrate (12). (See Fig. 3).

It would have been obvious to one having ordinary skill in the art at the time of the invention was made to form a doped region (26) below the termination of each isolation trench (360) within the semiconductor substrate (120) of Omid-Zohoor as taught by Lee to provide further electrical isolation effect between circuit components.

With respect to claim 21, Lee '316 further teaches forming a liner (50) prior to filling the isolation trench. (See Fig. 15).

It would have been obvious to one having ordinary skill in the art at the time of the invention was made to form the liner (50) upon the sidewall of each isolation trench prior to filling each isolation trench (360) of Omid-Zohoor as taught by Lee to release stress on the trench surface.

With respect to claim 22, the liner (50) of Lee is a thermally grown oxide of the semiconductor substrate (32).

15. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Omid-Zohoor '072 and Lee '316 as applied to claim 18 above, and further in view of Poon '540.

Omid-Zohoor and Lee are shown to teach all of the features of the claim with the exception of forming liner comprises deposition of a composition of matter.

However, Poon teaches forming liner (50) upon sidewall (24) of isolation trench (22) comprises deposition of a composition of matter. (See Fig. 11).

It would have been obvious to one having ordinary skill in the art at the time of the invention was made to form liner (50) of Lee '316 comprises deposition of a composition of matter as taught by Poon to protect the substrate from further oxidation.

16. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Omid-Zohoor '072 in view of Lee '316.

Omid-Zohoor teaches a method of forming a microelectronic structure substantially as claimed including:

forming an oxide layer (340) upon a semiconductor substrate (120);

forming a first dielectric layer (344) over the oxide layer;

selectively removing the first dielectric layer to expose the oxide layer at a plurality of areas;

forming a second dielectric layer (352) conformally over the oxide layer and the first dielectric layer;

selectively removing the second dielectric layer to form a plurality of spacers (356) from the second dielectric layer, wherein each the spacer is upon the oxide layer, is in contact with the first dielectric layer, and is adjacent to an area of the plurality of areas;

forming a plurality of isolation trenches (360) extending below the oxide layer into and terminating within the semiconductor substrate, wherein each the isolation trench is adjacent to and below a pair of the spacers and is situated at a corresponding area of the plurality of areas;

filling each isolation trench (360) with a conformal third layer (364), the conformal third layer extending above the oxide layer in contact with a corresponding pair of the spacers;

planarizing the conformal third layer to form therefrom an upper surface for each the isolation trench that is co-planar to the other the upper surfaces;

wherein material that is electrically insulative extends continuously between and within the plurality of isolation trenches;

wherein the upper surface for each the isolation trench is formed from the conformal third layer, the spacers, and the first dielectric layer; and

wherein the microelectronic structure is defined at least in part by the plurality of spacers, the conformal third layer, and the plurality of isolation trenches. (See Figs. 3A-M, col. 4, l. 1-col. 5, l. 4).

Thus, Omid-Zohoor is shown to teach all of the features of the claim with the exception of forming a polysilicon layer upon the oxide layer (340).

However, Lee teaches forming a polysilicon layer (36) between the oxide layer (34) and the first dielectric layer (38). (See Fig. 6).

It would have been obvious to one having ordinary skill in the art at the time of the invention was made to form a polysilicon layer (36) between the oxide layer (340) and the first dielectric layer (344) of Omid-Zohoor as taught by Lee to form an etch selectable layer that is differed form the oxide layer and the first dielectric layer.

17. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Omid-Zohoor '072 in view of Lee '316.

Omid-Zohoor teaches a method of forming a microelectronic structure substantially as claimed including:

forming an oxide layer (340) upon a semiconductor substrate (120);

forming a first dielectric layer (344) over the oxide layer;

selectively removing the first dielectric layer to expose the oxide layer at a plurality of areas;

forming a second dielectric layer (352) conformally over the oxide layer and the first dielectric layer;

selectively removing the second dielectric layer to form a plurality of spacers (356) from the second dielectric layer, wherein each the spacer is upon the oxide layer, is in contact with the first dielectric layer, and is adjacent to an area of the plurality of areas;

forming a plurality of isolation trenches (360) extending below the oxide layer into and terminating within the semiconductor substrate, wherein each the isolation trench is adjacent to and below a pair of the spacers and is situated at a corresponding area of the plurality of areas;

filling each isolation trench (360) with a conformal third layer (364), the conformal third layer extending above the oxide layer in contact with a corresponding pair of the spacers;

planarizing the conformal third layer to form therefrom an upper surface for each the isolation trench that is co-planar to the other the upper surfaces;

exposing the oxide layer upon a portion of a surface of the semiconductor substrate;

forming a gate oxide layer (380) upon the portion of the surface of the semiconductor substrate;

forming a layer composed of polysilicon (384) upon the gate oxide layer in contact with a pair of the spacers; and

selectively removing the third layer, the spacers and the layer composed of polysilicon to form a portion of at least one of the upper surfaces;

wherein material that is electrically insulative extends continuously between and within the plurality of isolation trenches. (See Figs. 3A-Q, col. 4, l. 1-col. 5, l. 23).

Thus, Omid-Zohoor is shown to teach all of the features of the claim with the exception of forming a polysilicon layer upon the oxide layer (340).

However, Lee teaches forming a polysilicon layer (36) between the oxide layer (34) and the first dielectric layer (38). (See Fig. 6).

It would have been obvious to one having ordinary skill in the art at the time of the invention was made to form a polysilicon layer (36) between the oxide layer (340) and the first dielectric layer (344) of Omid-Zohoor as taught by Lee to form an etch selectable layer that is differed from the oxide layer and the first dielectric layer.

As shown in Fig. 3Q, a portion of the polysilicon layer (384) is selectively removed.

18. Claims 26 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Omid-Zohoor '072 in view of Lee '316.

Omid-Zohoor teaches a method of forming a microelectronic structure substantially as claimed including:

forming an oxide layer (340) upon a semiconductor substrate (120);

forming a first dielectric layer (344) over the semiconductor substrate;

selectively removing the first dielectric layer to expose the oxide layer at a plurality of areas;

forming a second dielectric layer (352) conformally over the oxide layer and the first dielectric layer;

selectively removing the second dielectric layer to form a plurality of spacers (356) from the second dielectric layer, wherein each the spacer is upon the oxide layer, is in contact with the first dielectric layer, and is adjacent to an area of the plurality of areas;

forming a plurality of isolation trenches (360) extending below the oxide layer into and terminating within the semiconductor substrate, wherein each the isolation trench is adjacent to and below a pair of the spacers and is situated at a corresponding area of the plurality of areas;

filling each the isolation trench with a conformal third layer (364), the conformal third layer extending above the oxide layer in contact with a corresponding pair of the spacers;

planarizing the conformal third layer by an etch using etch recipe to form therefrom an upper surface for each the isolation trench that is co-planar to the other the upper surfaces;

wherein material that is electrically insulative extends continuously between and within the plurality of isolation trenches; and

wherein the microelectronic structure is defined at least in part by the plurality of spacers, the conformal third layer and the plurality of isolation trenches. (See Figs. 3A-M, col. 4, l. 1-col. 5, l. 4).

Thus, Omid-Zohoor is shown to teach all of the features of the claim with the exception of forming a polysilicon layer upon the oxide layer (340).

However, Lee teaches forming a polysilicon layer (36) therebetween the oxide layer (34) and the first dielectric layer (38). (See Fig. 6).

It would have been obvious to one having ordinary skill in the art at the time of the invention was made to form a polysilicon layer (36) between the oxide layer (340) and the first dielectric layer (344) of Omid-Zohoor as taught by Lee to form an etch selectable layer that is differed from the oxide layer and the first dielectric layer.

Regarding the etch recipe, it appears that the etch recipe of Lee '316 is within the claimed range of the present claim because the etching results in an upper surface for each the isolation trench that is co-planar to the other the upper surfaces. (See Fig. 9).

With respect to claim 27, the etch ratio of Lee '316 appears to be within the claimed range.

Within purview of one having ordinary skill in the art, it would have been obvious to determine the optimum etch ratio of the layers. See *In re Aller*, Lacey and Hall (10 USPQ 233-237) "It is not inventive to discover optimum or workable ranges by routine experimentation."

19. Claims 28-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Omid-Zohoor '072 in view of Lee '316.

Omid-Zohoor teaches a method of forming a microelectronic structure substantially as claimed including:

forming an oxide layer (340) upon a semiconductor substrate (120);

forming a first dielectric layer (344) over the semiconductor substrate;

selectively removing the first dielectric layer to expose the oxide layer at a plurality of areas;

forming a second dielectric layer (352) conformally over the oxide layer and the first dielectric layer;

selectively removing the second dielectric layer to form a plurality of spacers (356) from the second dielectric layer, wherein each the spacer is upon the oxide layer, is in contact with the first dielectric layer, and is adjacent to an area of the plurality of areas;

forming a plurality of isolation trenches (360) extending below the oxide layer into and terminating within the semiconductor substrate, wherein each the isolation trench is adjacent to and below a pair of the spacers and is situated at a corresponding area of the plurality of areas;

filling each the isolation trench with a conformal third layer (364), the conformal third layer extending above the oxide layer in contact with a corresponding pair of the spacers;

planarizing the conformal third layer to form therefrom an upper surface for each the isolation trench that is co-planar to the other the upper surfaces;

chemical mechanical planarizing the conformal third layer (364), the spacers and the first dielectric layer (344) to form a planar first upper surface; and

etching to forms a planar second upper surface, the second upper surface being situated above the oxide layer;

wherein material that is electrically insulative extends continuously between and within the plurality of isolation trenches. (See Figs. 3A-N, col. 4, l. 1-col. 5, l. 4).

Thus, Omid-Zohoor is shown to teach all of the features of the claim with the exception of forming a polysilicon layer upon the oxide layer (340).

However, Lee teaches forming a polysilicon layer (36) therebetween the oxide layer (34) and the first dielectric layer (38). (See Fig. 6).

It would have been obvious to one having ordinary skill in the art at the time of the invention was made to form a polysilicon layer (36) between the oxide layer (340) and the first dielectric layer (344) of Omid-Zohoor as taught by Lee to form an etch selectable layer that is differed form the oxide layer and the first dielectric layer.

With respect to claims 29 and 30, it appears that the etch recipe of Lee '316 is within the claimed range of the present claim because the etching results in an upper surface for each the isolation trench that is co-planar to the other the upper surfaces. (See Fig. 9).

Within purview of one having ordinary skill in the art, it would have been obvious to determine the optimum etch ratio of the layers. See *In re Aller*, Lacey and Hall (10 USPQ 233-237) "It is not inventive to discover optimum or workable ranges by routine experimentation."

20. Claims 31, 32 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Omid-Zohoor '072 in view of Lee '316.

Omid-Zohoor teaches a method of forming a microelectronic structure substantially as claimed including:

forming a pad oxide layer (340) upon a semiconductor substrate (120);

forming a silicon nitride layer (344) over semiconductor substrate;

selectively removing the silicon nitride layer to expose the oxide layer at a plurality of areas;

forming a first silicon dioxide layer (352) conformally over the oxide layer and the silicon nitride layer;

selectively removing the first silicon dioxide layer to form a plurality of spacers (356) from the first silicon dioxide layer, wherein each the spacer is upon the pad oxide layer, is in contact with the silicon nitride layer, and is adjacent to an area of the plurality of areas;

forming a plurality of isolation trenches (360) extending below the pad oxide layer into and terminating within the semiconductor substrate, wherein each the isolation

trench is adjacent to and below a pair of the spacers and is situated at a corresponding area of the plurality of areas;

filling each isolation trench (360) with a second layer (364), the second layer extending above the oxide layer in contact with a corresponding pair of the spacers; and

planarizing the second layer and each spacer to form therefrom an upper surface for each isolation trench that is co-planar to the other upper surfaces and is situated above the pad oxide layer;

wherein material that is electrically insulative extends continuously between and within the plurality of isolation trenches. (See Figs. 3A-M, col. 4, l. 1-col. 5, l. 4).

Thus, Omid-Zohoor is shown to teach all of the features of the claim with the exception of forming a polysilicon layer upon the oxide layer (340), the doped region below each isolation trench and forming a liner on the sidewall of the trench.

However, Lee teaches forming a polysilicon layer (36) between the oxide layer (34) and the first dielectric layer (38). (See Fig. 6).

It would have been obvious to one having ordinary skill in the art at the time of the invention was made to form a polysilicon layer (36) between the oxide layer (340) and the first dielectric layer (344) of Omid-Zohoor as taught by Lee to form an etch selectable layer that is differed form the oxide layer and the first dielectric layer.

Lee, further, teaches forming a corresponding doped region (26) below the termination trench within the semiconductor substrate (12). (See Fig. 3).

It would have been obvious to one having ordinary skill in the art at the time of the invention was made to form a doped region (26) below the termination of each isolation trench (360) within the semiconductor substrate (120) of Omid-Zohoor as taught by Lee to provide further electrical isolation effect between circuit components.

Additionally, Lee teaches forming a liner (24) upon the sidewall of each isolation trench, extending from an interface thereof with the pad oxide layer (14) to the termination of the isolation trench (22) within the semiconductor substrate (12). (See Fig. 3).

It would have been obvious to one having ordinary skill in the art at the time of the invention was made to form the liner (24) upon the sidewall of each isolation trench prior to filling each isolation trench (360) of Omid-Zohoor as taught by Lee to release stress on the trench surface.

With respect to claim 32, as best understood by examiner, the liner (24) of Lee is thermally grown oxide of the semiconductor substrate, and wherein the second layer (42a) of Lee '316 is composed of an electrically conductive material. (See Fig. 16).

With respect to claim 34, the method of Omid-Zohoor further includes:

exposing the pad oxide layer (340) upon a portion of a surface of the semiconductor substrate (120);

forming a gate oxide layer (380) upon the portion of the semiconductor substrate; and

forming a layer (384) composed of polysilicon upon the gate oxide layer (380) in contact with a pair of the spacers; and

selectively removing the layer composed of polysilicon to form a portion of at least one of the upper surface. (See Fig. 3Q).

21. Claim 33 is rejected under 35 U.S.C. 103(a) as being unpatentable over Omid-Zohoor '072 and Lee '316 as applied to claim 31 above, and further in view of Poon '540.

Omid-Zohoor '072 and Lee '316 are shown to teach all of the features of the claim with the exception of forming liner (24) composed of silicon nitride.

However, Poon teaches forming liner (50) comprises silicon nitride upon the isolation trench (22).

It would have been obvious to one having ordinary skill in the art at the time of the invention was made to form liner (24) of Oim-Zohoor, in view of Lee '316, comprises silicon nitride (50) as taught by Poon '540 to protect the substrate from further oxidizing.

22. Claims 35-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Omid-Zohoor '072 in view of Lee '316.

Omid-Zohoor teaches a method of forming a microelectronic structure substantially as claimed including:

providing a semiconductor substrate (120) having a top surface with an oxide layer (340) thereon;

forming a first layer over the semiconductor substrate;

forming a plurality of isolation trenches having electrically insulative material (364) extending continuously between and within the plurality of isolation trenches, each isolation trench:

- having a spacer (356) composed of a dielectric material upon the oxide layer in contact with the first layer;
- extending from an opening thereto at the top surface of the semiconductor substrate and below the oxide layer into and terminating within the semiconductor substrate adjacent to and below the spacer;
- having a second layer (364) filling the isolation trench and extending above the oxide layer in contact with the spacer; and
- having a planar upper surface formed from the second layer and the spacer and being situated above the oxide layer; and

wherein the microelectronic structure is defined at least in part by the plurality of spacers, the second layer, and the plurality of isolation trenches. (See Figs. 3A-M, col. 4, l. 1-col. 5, l. 4).

Thus, Omid-Zohoor is shown to teach all of the features of the claim with the exception of forming a polysilicon layer upon the oxide layer (340).

However, Lee teaches forming a polysilicon layer (36) between the oxide layer (34) and the first dielectric layer (38). (See Fig. 6).

It would have been obvious to one having ordinary skill in the art at the time of the invention was made to form a polysilicon layer (36) between the oxide layer (340) and the first dielectric layer (344) of Omid-Zohoor as taught by Lee to form an etch selectable layer that is differed form the oxide layer and the first dielectric layer.

With respect to claim 36, Lee '316 further teaches:

doping the semiconductor substrate with a dopant having a first conductivity type;

doping the semiconductor substrate (12) below each isolation trench with a dopant having a second conductivity type opposite the first conductivity type to form a doped trench bottom that is below and in contact with a respective one of each isolation trench. (See Fig. 3).

It would have been obvious to one having ordinary skill in the art at the time of the invention was made to form a doped region (26) below the termination of each isolation trench (360) within the semiconductor substrate (120) of Omid-Zohoor as taught by Lee to provide further electrical isolation effect between circuit components.

With respect to claim 37, the doped trench bottom (26) of Lee '316 has a width, each isolation trench(22) has a width, and the width of each doped trench bottom is greater than the width of the respective isolation trench. (See Fig. 3).

23. Claims 39 and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Omid-Zohoor '072 as applied to claim 38 above, and further in view of Lee '316.

Omid-Zohoor is shown to teach all of the features of the claim with the exception of doping of the semiconductor substrate.

However, Lee '316 teaches:

doping the semiconductor substrate with a dopant having a first conductivity type;
doping the semiconductor substrate (12) below each isolation trench with a dopant having a second conductivity type opposite the first conductivity type to form a doped trench bottom that is below and in contact with a respective one of each isolation trench. (See Fig. 3).

It would have been obvious to one having ordinary skill in the art at the time of the invention was made to form a doped region (26) below the termination of each isolation trench (360) within the semiconductor substrate (120) of Omid-Zohoor as taught by Lee to provide further electrical isolation effect between circuit components.

With respect to claim 40, the doped trench bottom (26) of Lee '316 has a width, each isolation trench(22) has a width, and the width of each doped trench bottom is greater than the width of the respective isolation trench. (See Fig. 3).

24. Claim 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Omid-Zohoor '072 in view of Lee '316.

Omid-Zohoor teaches a method of forming a microelectronic structure substantially as claimed including:

providing a semiconductor substrate (120) having a top surface with an oxide layer (340) thereon;

forming a first layer (344) over the semiconductor substrate;

forming a first isolation structure including:

a first spacer (356) composed of a dielectric material upon the oxide layer in contact with the first layer;

a first isolation trench (360) extending from an opening thereto at the top surface of the semiconductor substrate and below the oxide layer into and terminating within the semiconductor substrate adjacent to and below the first spacer, wherein the first spacer is situated on a side of the first isolation trench;

a second spacer (356) composed of a dielectric material upon the oxide layer in contact with the first layer, the second spacer being situated on a side of the first isolation trench opposite the side of the first spacer;

forming a second isolation structure including:

a first spacer (356) composed of a dielectric material upon the oxide layer in contact with the first layer;

a first isolation trench (360) extending below the oxide layer into and terminating within the semiconductor substrate adjacent to and below the first spacer of the second isolation structure, wherein the first spacer of the second isolation structure is situated on a side of the first isolation trench;

a second spacer (356) composed of a dielectric material upon the oxide layer in contact with the first layer and the polysilicon layer, the second spacer of the second isolation structure being situated on a side of the first isolation trench opposite the side of the first spacer of the second isolation structure;

forming an active area located within the semiconductor substrate between the first and second isolation structures;

forming a second layer (364), composed of an electrically insulative material, filling the first and second isolation trenches and extending continuously therebetween and above the oxide layer in contact with the first and second spacers of the respective first and second isolation structures; and

forming a planar upper surface from the second layer and the first and second spacers of the respective first and second isolation structures, and being situated above the oxide layer; and

wherein the microelectronic structure is defined at least in part by the active area, the second layer and the first and second isolation trenches. (See Figs. 3A-M, col. 4, l. 1-col. 5, l. 4).

Thus, Omid-Zohoor is shown to teach all of the features of the claim with the exception of forming a polysilicon layer upon the oxide layer (340).

However, Lee teaches forming a polysilicon layer (36) between the oxide layer (34) and the first dielectric layer (38). (See Fig. 6).

It would have been obvious to one having ordinary skill in the art at the time of the invention was made to form a polysilicon layer (36) between the oxide layer (340) and the first dielectric layer (344) of Omid-Zohoor as taught by Lee to form an etch selectable layer that is differed from the oxide layer and the first dielectric layer.

Response to Arguments

25. Applicant's arguments with respect to claims 1-43 have been considered but are moot in view of the new ground(s) of rejection.


Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh D. Mai whose telephone number is (703) 305-0575. The examiner can normally be reached on 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (703) 306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Anh D. Mai
August 17, 2000


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